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An Overview of Different Multi-level Inverters

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Abstract: **The output voltage of an inverter has in general non-sinusoidal shape. The required AC output quantity – frequency and voltage – is created by a sequence of segments properly cut out from the input variable quantity, which is a DC-voltage. The required output quantities, AC voltage amplitude and frequency, are created either from rectangular pulses or by the pulse-width- modulation (PWM).Power source with a non-sinusoidal voltage applied to a electric equipment brings some undesirable effects. For example, it can cause additional losses in the windings and ferromagnetic circuits of transformers. In AC motors the additional losses are higher and operating characteristics of motors are worse. In photovoltaic power sources, the use of inverters must be carefully considered, because a wide range of harmonics can be generated. This would greatly decline the quality of produced and transmitted electric energy. Demand for high-voltage, high power converters capable of producing of producing high-quality waveform while utilizing low voltage devices and reduced switching frequency has led to the multilevel inverter development with regard to semiconductor power switch voltage limit.In this paper an overview is presented of different Multilevel inverter techniques to reduce the total harmonic distortion of output voltage in a inverter.**

Keywords: **Harmonic distortion , H-bridge inverter ,Diode-clamped inverter, Flying-capacitor inverter , Cascaded H-bridge inverter.**

1. INTRODUCTION

The voltage source inverters produce an output voltage or current with levels either 0 or ± V_{dc}. They are known as the two-level inverter. To obtain the quality output voltage or a current waveform with a minimum amount of ripple content, they require high-switching frequency along with various pulse-width modulation (PWM) strategies. In high-power and high-voltage applications, these two-level inverters, however, have some limitations in operating at high frequency mainly due to switching losses and constraints of device ratings. Moreover, the semiconductor switching devices should be used in such a manner as to avoid problems associated with their series-parallel combinations that are necessary to obtain capability of handling high voltages and currents.

Demand for high-voltage, high-power converters capable of producing high-quality waveforms while utilizing low voltage devices and reduced switching frequencies has led to multilevel inverter development with regard to semiconductor power switch voltage limits. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the ouput of which generate voltages with stepped waveforms. The commutation of switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages.

The general structure of the multilevel inverter is to synthesize a near sinusoidal voltage from several levels of dc voltages. As the number of levels increases, the synthesized output waveform has more steps, which produce a staircase wave that approaches a desired waveform. Also, as more steps are added to the waveform, the harmonic distortion of the output wave decreases, approaching zero as the number of levels increases.

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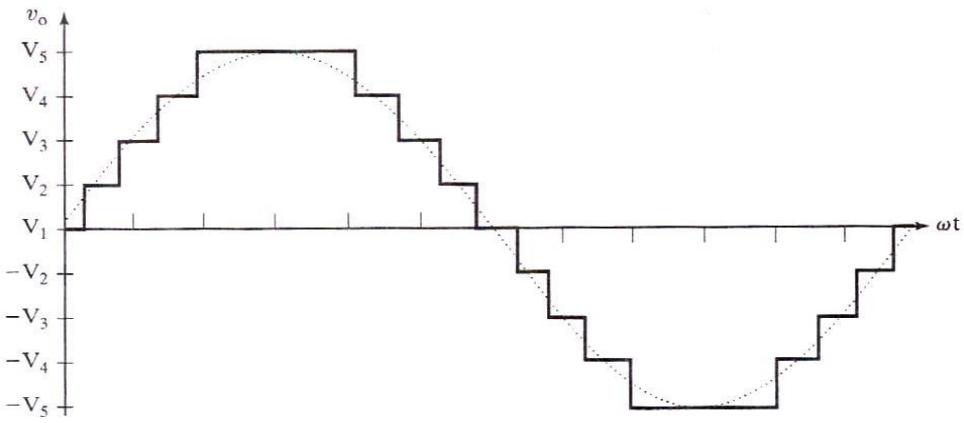

Fig.1: Staircase multilevel output voltage

The multilevel inverters can be classified into three types:

1. Diode - clamped multilevel inverter
2. Flying - capacitor multilevel inverter
3. Cascade multilevel inverter

II. DIODE-CLAMPED MULTILEVEL INVERTER

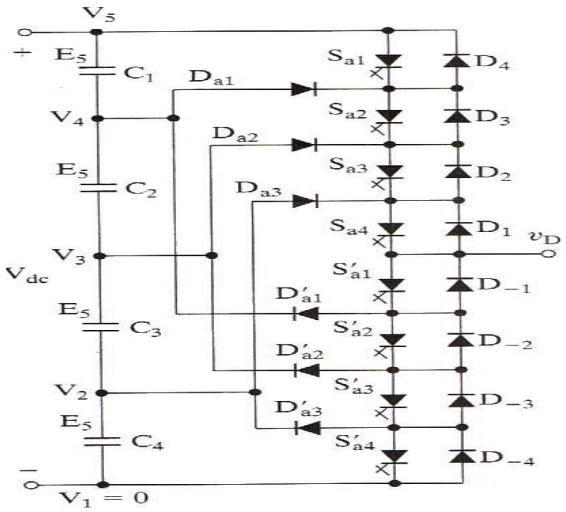

Fig.2: One leg of Diode clamped inverter

A diode-clamped multilevel (m-level) inverter (DCMLI) consists of (m-1) capacitors on the dc bus and produces m levels on the phase voltage. Fig.2 shows one leg and a full-bridge five-level diode-clamped inverter.

- The DC bus consists of four capacitors C_1 , C_2 , C_3 and C_4.
- For a DC bus voltage V_{dc}, the voltage across each capacitor is V_{dc}/4, and each device voltage stress is limited to one capacitor voltage level V_{dc}/4 through clamping diodes.
- An m-level inverter leg requires (m-1) capacitors, 2(m-1) switching devices and (m-1)(m-2) clamping diodes.

The steps to synthesize the staircase five-level output voltage are as follows:

i. For an output voltage level $V_{ao} = V_{dc}$, turn on all upper-half switches S_{a1} to S_{a4}.

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ii. For an output voltage level $V_{ao} = \frac{3}{4}V_{dc}$, turn on three upper-half switches S_{a2} to S_{a4} and one lower switch S'_{a1}.

iii. For an output voltage level $V_{ao} = \frac{1}{2}V_{dc}$, turn on two upper-half switches S_{a3} and S_{a4} and two lower switch S'_{a1} and S'_{a2}.

iv. For an output voltage level $V_{ao} = \frac{1}{4}V_{dc}$, turn on one upper-half switch S_{a4} and three lower switch S'_{a1} , S'_{a2} and S'_{a3}.

v. For an output voltage level $V_{ao} = 0$, turn on all lower-half switches S'_{a1} S'_{a2} , S'_{a3} and S'_{a4}.

The major advantages of the diode-clamped inverter can be summarized as follows:

i. When the number of levels is high enough, the harmonic content is low enough to avoid the need for filters.

ii. Inverter efficiency is high because all devices are switched at the fundamental frequency.

iii. The control method is simple.

The major disadvantages of the diode-clamped inverter can be summarized as follows:

i. Excessive clamping diodes are required when the number of levels is high.

ii. It is difficult to control the real power flow of the individual inverter in multilevel system.

III. FLYING-CAPACITOR MULTILEVEL INVERTER

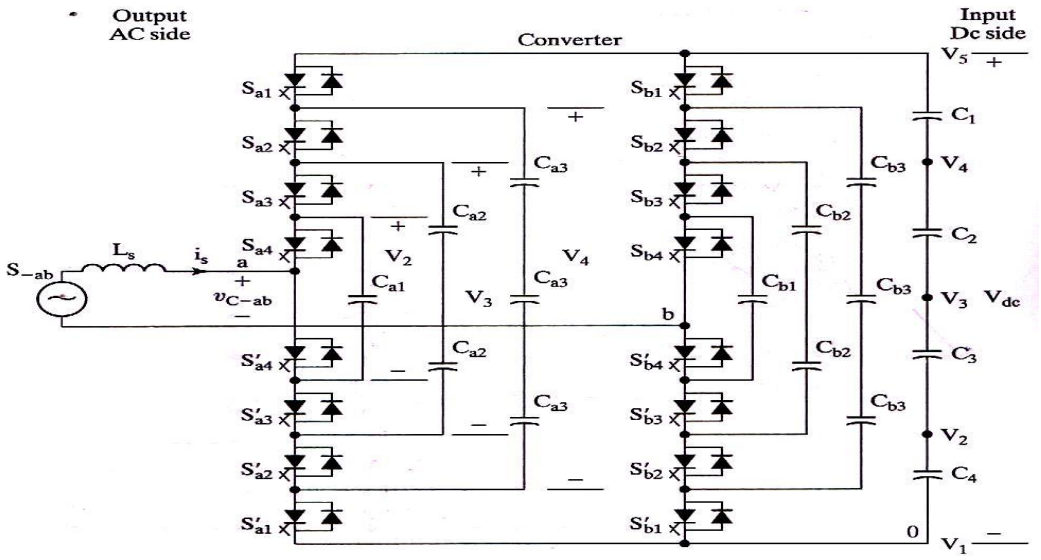

Fig.3: 5-level Flying capacitor inverter

Fig 3 shows a single-phase, full-bridge, five-level, flying-capacitor multilevel inverter (FCMLI).

I. The numbering order of the switches is S_{a1} , S_{a2} , S_{a3} , S_{a4} , S'_{a1} , S'_{a2} and S'_{a3} and S'_{a4} . The order of switches is different than the diode-clamped inverter.

II. The numbering is immaterial as long as the switches are turned on and off in the right sequence to produce the desired output.

III. Each phase leg has an identical structure. Assuming that each capacitor has the same voltage rating, the series connection of the capacitor indicates the voltage level between the clamping points.

IV. Three inner-loop balancing capacitors (C_{a1} , C_{a2} and C_{a3}) for phase-leg a are independent from those for phase-leg b. All phase legs share the same dc-link capacitors C_1 through C_4 .

The voltage level for the flying-capacitors inverter is similar to that of the diode-clamped type of inverter. That is, in a m-level inverter phase voltage has m levels and line voltage has (2m-1) level .

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IV. CASCADED H-BRIDGE MULTILEVEL INVERTER

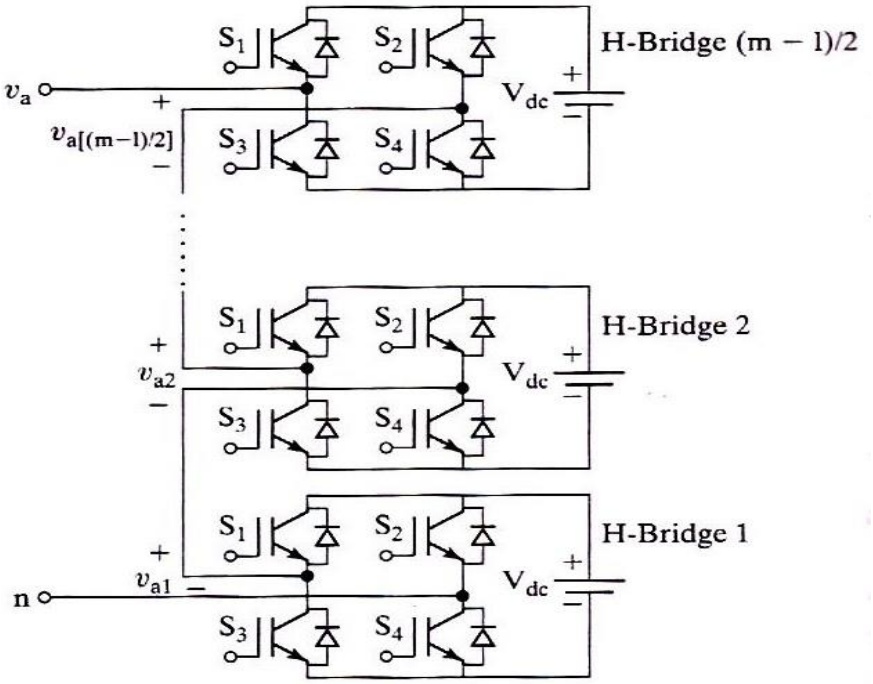

Fig.4: Cascaded H-bridge m-level inverter

Fig. 4 shows the generalised m-level cascaded H-bridge multilevel inverter. The phase output voltage is synthesized by the sum of each inverter outputs

$$V_{an} = V_{a1} + V_{a2} \ldots\ldots + V_{a\,(m-1)/2}$$

To synthesize a multilevel waveform, the AC output of each of the different level H-bridge cells are connected in series. The cascaded voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels in a cascaded inverter is defined by

N = 2S + 1

Where S is the number of dc sources.

Controlling the conduction angles at different inverter levels can minimise the harmonic distortion of the output voltage. The output voltage of the inverter is almost sinusoidal, and it has less than 5% total harmonic distortion (THD) with each of the H-bridges switching only at fundamental frequency.

A five-level output phase voltage waveform can be obtained with two separate dc sources and two H-bridge cells. Each inverter level can generate three different voltage outputs $+V_{dc}$, $-V_{dc}$ and 0, by connecting the dc source to the output side by different combinations of the four switches S1, S2, S3 and S4.

Using the top level as the example, turning on S1 & S2 yields $V_{a4} = +V_{dc}$. Turning on S3 & S4 yields $V_{a4} = -V_{dc}$. Turning off all the switches yields $V_4 = 0$. Similarly, the ac output voltage at each level can be obtained in the same manner.

The output voltage of a single phase seven level cascaded H-bridge inverter can be obtained from 3 H-bridge cells with 3 SDCSs.

Similarly a 9-level output can be obtained from 4 H-bridge cells and 4 separate SDCSs. Because zero voltage is common for all inverter outputs, the total level of output voltage waveform becomes 2S+1. Phase voltage waveform for a nine-level cascaded inverter and all H-bridge cell output waveforms are shown in fig. 5.

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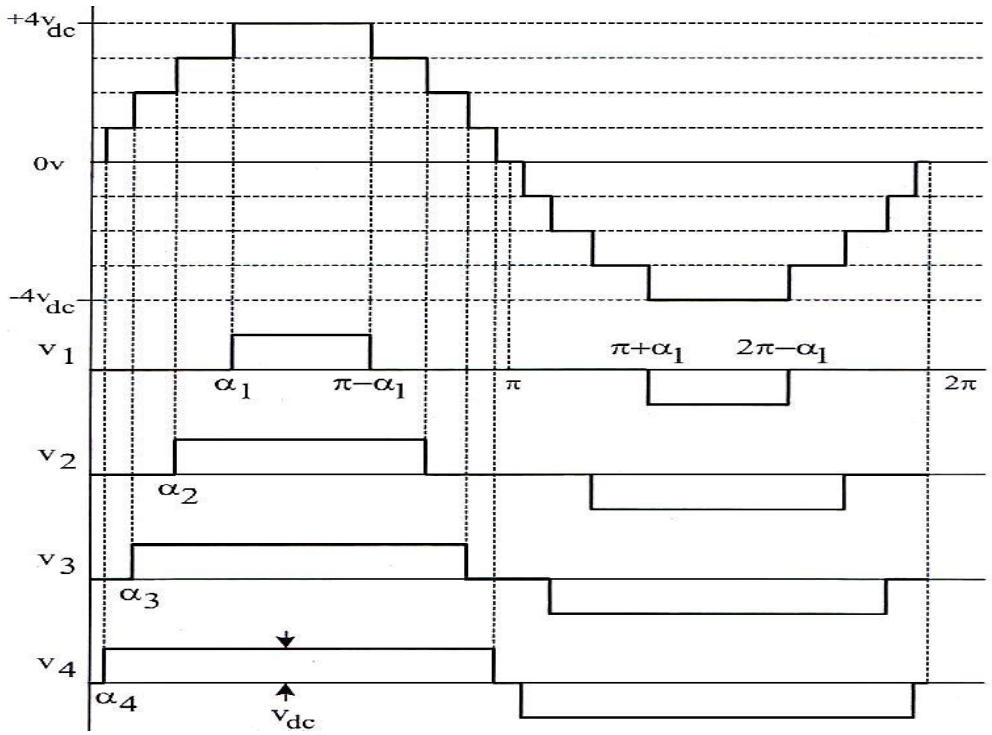

Fig.5 Nine-level output voltage waveform

V. COMPARISON OF MULTILEVEL INVERTER

A table given below compares the omponent requirements per phase leg among the three multilevel converters. All devices are assumed to have the same voltage rating, but not necessarily the same current rating **.**

INVETER COMPONENTS	DIODE-CLAMPED	FLYING-CAPACITOR	CASCADED INVERTER
Main switching devices	(m – 1) x 2	(m – 1) x 2	(m – 1) x 2
Main diodes	(m – 1) x 2	(m – 1) x 2	(m – 1) x 2
Clamping diodes	(m – 1) x (m – 2)	0	0
Dc bus capacitor	(m – 1)	(m – 1)	(m – 1) / 2
Balancing capacitors	0	(m – 1) x (m – 2)/2	0

VI. CONCLUSION

The cascaded inverter requires the least number of components and has the potential for utility interface applications because of its capabilities for applying modulation and soft-switching techniques.

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